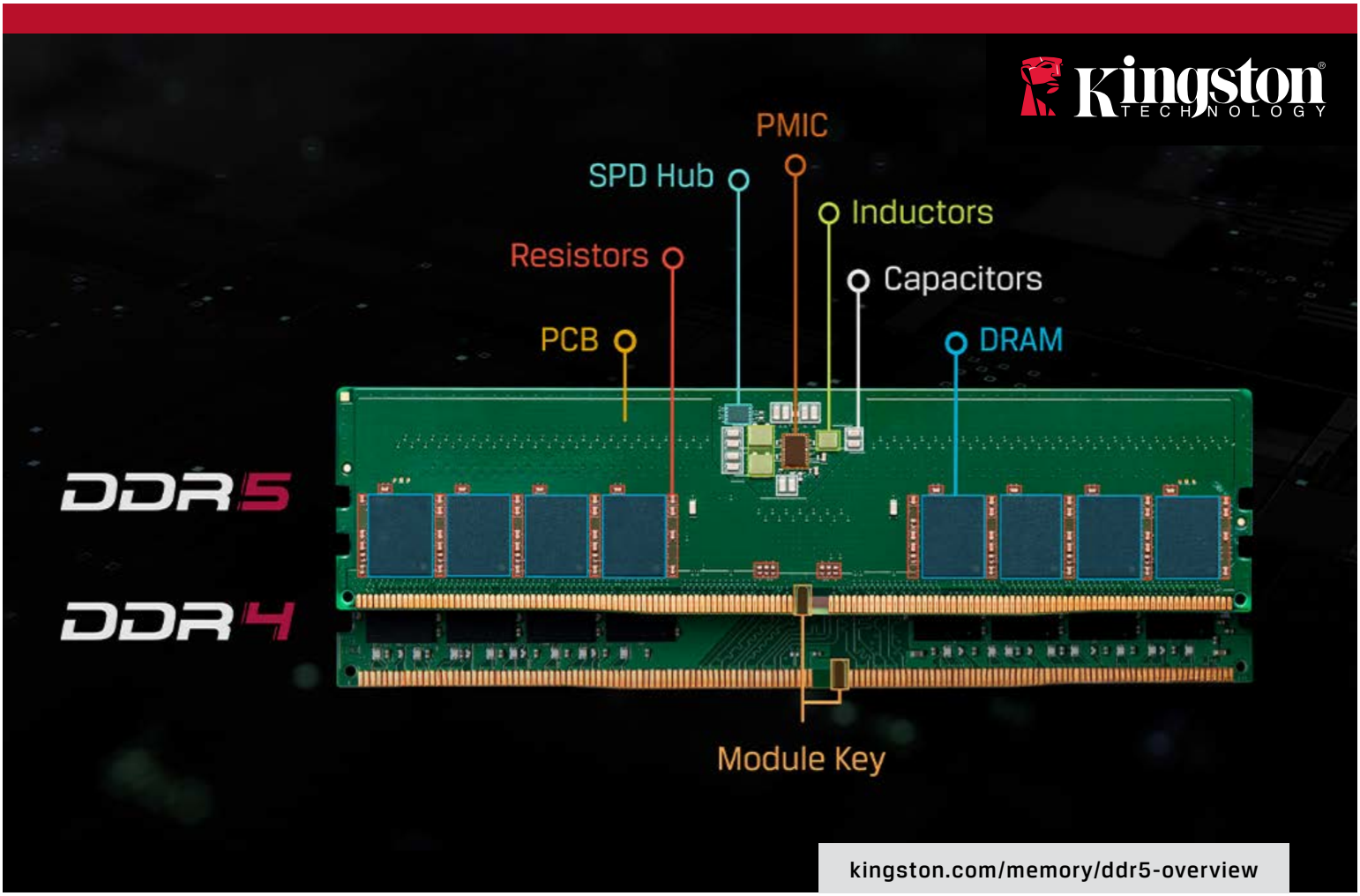

DDR5 Memory Standard

An introduction to the next generation of DRAM module technology

DDR5 is the 5th generation of Double Data Rate Synchronous Dynamic Random Access Memory, aka DDR5 SDRAM. It began in 2017 by the industry standards body JEDEC (Joint Electron Device Engineering Council) with input from the leading global memory semiconductor and chipset architecture vendors, including Kingston, DDR5 is designed with new features for higher performance, lower power, and more robust data integrity for the next decade of computing. DDR5 debuted in 2021.

GREATER STARTING SPEED PERFORMANCE

DDR5 debuts at 4800MT/s, while DDR4 tops out at 3200MT/s, a 50% increase in bandwidth. In cadence with compute platform releases, DDR5 has planned performance increases that will scale to 6400MT/s.

REDUCED POWER / INCREASED EFFICIENCY

At 1.1V, DDR5 consumes ~20% less power than DDR4 equivalent components at 1.2V. While conserving battery life in laptops, it also has a significant advantage for enterprise servers working around the clock.

PMIC

DDR5 modules feature on-board Power Management Integrate Circuits (PMIC), which help regulate the power required by the various components of the memory module (DRAM, Register, SPD hub, etc). For server class modules the PMIC uses 12V, and for PC class modules the PMIC uses 5V. This makes for better power distribution than previous generations, improves signal integrity, and reduces noise.

SPD HUB

DDR5 utilizes a new device integrating the Serial Presence Detect (SPD) EEPROM with additional hub features, managing access to the external controller and decoupling the memory load on the internal bus from external.

DUAL 32-BIT SUBCHANNELS

DDR5 splits the memory module into two independent 32-bit addressable subchannels to increase efficiency and lower the latencies of data accesses for the memory controller. The data width of the DDR5 module is still 64-bit, however breaking it down into two 32-bit addressable channels increases overall performance. For server class memory (RDIMMs), 8-bits are added to each subchannel for ECC support for a total of 40-bits per subchannel, or 80-bits per Rank. Dual Rank modules feature four 32-bit subchannels.

MODULE KEY

The notch in the center of the module acts like a key, aligning with DDR5 sockets to prevent DDR4, DDR3, or other unsupported module types from being installed. Unlike DDR4, DDR5 module keys differ between module types: UDIMM and RDIMM.

ON-DIE ECC

On-Die ECC (Error Correction Code) is a new feature designed to correct bit errors within the DRAM chip. As DRAM chips increase in density through shrinking wafer lithography, potential for data leakage increases. On-Die ECC mitigates this risk by correcting errors within the chip, increasing reliability and reducing defect rates. This technology cannot correct errors outside of the chip or that occur on the bus between the module and memory controller housed within the CPU. ECC enabled processors for servers and workstations feature the coding that can correct single or multi-bit errors on the fly. Extra DRAM bits must be available to allow this correction to occur, featured on ECC class module types like ECC unbuffered, Registered, and

Load Reduced.

ADDITIONAL TEMPERATURE SENSORS

Server class DDR5 RDIMMs and LRDIMMs add temperature sensors to the ends of the modules to monitor thermal conditions across the length of the DIMM. This allows for more precise control of system cooling, as opposed to throttling performance seen in DDR4 for high temperatures.

INCREASED BANKS AND BURST LENGTH

DDR5 doubles the banks from 16 to 32. This allows for more pages to be open at a time, increasing efficiency. Also doubled is the minimum burst length to 16, up from 8 for DDR4. This improves data bus efficiency, providing twice the data on the bus, and consequently reduces the number of reads/writes to access the same cache data line.

IMPROVED REFRESHES

DDR5 adds a new command called SAME-BANK Refresh, which allows a refresh of just one bank per bank group, versus all banks. When compared to DDR4, this command allows DDR5 to further improve on performance and efficiency.

DECISION FEEDBACK EQUALIZATION (DFE)

DDR5 utilizes Decision Feedback Equalization (DFE) to provide stable, reliable signal integrity on the module, required for high bandwidth.

more ⟩⟩

FORM FACTORS

While the memory modules themselves appear similar to DDR4, there are significant changes that make them incompatible with legacy systems. The key location (notch in the center) moves to prevent them from being installed into incompatible sockets.

- DIMM: 288-pins
- SODIMM: 262-pins
- Registered DIMMs
- Load Reduced DIMMs
- ECC Unbuffered DIMMs
- ECC Unbuffered SODIMMs
- Non-ECC Unbuffered DIMMs
- Non-ECC Unbuffered SODIMMs

JEDEC INDUSTRY STANDARD SPECIFICATIONS

Description		DDR5
Data Rates (Speed in MT/s)		4000, 4400, 4800, 5200, 5600, 6000, 6400 MT/s
Monolithic DRAM Densities (Gbit)		8Gb, 16Gb, 24Gb, 32Gb, 48Gb, 64Gb
Package Type and Ballout (x4, x8 / x16)		BGA, 3DS TSV (78, 82 / 102)
Interface	Voltage (VDD / VDDQ / VPP)	1.1 / 1.1 / 1.8 V
	Internal VREF	VREFDQ, VREFCA, VREFCS
	Command/Address	POD (Pseudo Open Drain)
	Equalization	DFE (Dynamic Feedback Equalization)
	Burst Length	BL16 / BC8 / BL32 (optional)
Core Architecture	Number of Banks	32 Banks (8 Bank Groups) 8 BG x 4 banks (16-64Gb x4/x8) 8 BG x 2 banks (8Gb x4/x8) 16 Banks (4 Bank Groups) 4 BG x 4 banks (16-64Gb x16) 4 BG x 2 banks (8Gb x16)
	Page Size (x4 / x8 / x16)	1KB / 1KB / 2KB
	Prefetch	16n
	DCA (Duty Cycle Adjustment)	DQS and DQ
	Internal DQS Delay Monitoring	DQS interval oscillator
	ODECC (On-die ECC)	128b+8b SEC error check and scrub
	CRC (Cyclic Redundancy Check)	Read/Write
	ODT (On-die Termination)	DQ, DQS, DM, CA bus
	MIR ("Mirror" pin)	Yes
	Bus Inversion	Command/address inversion (CAI)
	CA Training, CS Training	CA training, CS training
	Write Leveling Training Modes	Improved
	Read Training Patterns	Dedicated MRs for user-defined serial, clock, and LFSR -generated training patterns
	Mode registers	Up to 256 x 8 bits
	PRECHARGE Commands	All bank, per bank, and same bank
	REFRESH Commands	All bank and same bank
	Loopback Mode	Yes

MT/s denotes megatransfers (million transfers) per second and represents the effective data rate (speed) of DDR (Double Data Rate) SDRAM memory in computing. A DDR SDRAM memory module transfers data on the rise and fall of every clock cycle (1 Hz).

Ex: DDR4-3200 (PC4-3200)

Clock Rate: 1600MHz

Data Rate: 3200MT/s

Bandwidth: 25,600 MB/s (25.6 GB/s)