kingston.com/embedded

DRAM

Kingston LPDDR4 DRAM for embedded applications

Kingston discrete LPDDR4 DRAM is designed to meet the needs of embedded applications and offers a high-speed option with lower power consumption.

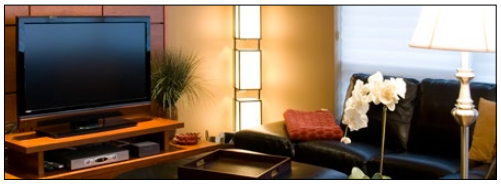
MARKET SEGMENTS

Industrial IoT / Robotics & Factory Automation

5G Networking/Telecommunications Communication Modules (WiFi Routers and Mesh Devices)

Office Equipment, Medical Devices, ATM, Vending Machines

Mobile Applications, Handheld



Smart Home (Sound Bars, Thermostats, Fitness Equipment, Vacuums, Beds, Faucets)

Smart City (HVAC, Lighting, Power Monitoring/ Metering, Parking Meters)

LPDDR4 PART NUMBERS AND SPECIFICATIONS

COMMERCIAL TEMPERATURE

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D0811PM2FDGUK	8Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x1.0	512Mx16	3733 Mbps	1.1V	-25°C ~ +85°C
B1621PM2FDGUK	16Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x1.0	512Mx32	3733 Mbps	1.1V	-25°C ~ +85°C

INDUSTRIAL TEMPERATURE

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D0811PM2FDGUKW	8Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x1.0	512Mx16	3733 Mbps	1.1V	-40°C ~ +95°C
B1621PM2FDGUKW	16Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x1.0	512Mx32	3733 Mbps	1.1V	-40°C ~ +95°C

KEY FEATURES

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Data mask (DM) write data-in at the both rising and falling edges of the data strobe
- Write Cycle Redundancy Code (CRC) is supported
- Programmable preamble for read and write is supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Driver strength selected by MRS
- Dynamic On Die Termination supported
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- This product in compliance with the RoHS directive
- Internal Vref DQ level generation is available
- TCAR (Temperature Controlled Auto Refresh) mode is supported
- LP ASR (Low Power Auto Self Refresh) mode is supported
- Command Address (CA) Parity (command/address) mode is supported
- Per DRAM Addressability (PDA)
- Fine granularity refresh is supported
- Geardown Mode(1/2 rate, 1/4 rate) is supported
- Self Refresh Abort is supported
- Maximum power saving mode is supported
- Banks Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- DMI pin support for write data masking and DBIdc functionality
- Low power consumption
- Per Bank Refresh
- Fully compliant with the JEDEC Low Power double Data Rate 4 (LPDDR4) Specification
- Partial Array Self-Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self-Refresh
  - (ATCSR) by built-in temperature sensor
  - All bank auto refresh and directed per bank auto refresh supported
- Double-data-rate architecture; two data transfers per one clock cycle
- Differential clock inputs (CK_t and CK_c) Bi-directional differential data strobe (DQS_tandDQS_c) Commands entered on both rising and falling CK_t edge; data and data mask referenced to both edges of DQS_t
- DMI pin support for write data masking and DBIdc functionality