Kingston DDR3/3L DRAM for embedded applications

Kingston on-board DRAM is designed to meet the needs of embedded applications and offers a low-voltage option for lower power consumption.

**DDR3/3L Part Numbers and Specifications**

<table>
<thead>
<tr>
<th>30nm DDR3/3L Part Number</th>
<th>Capacity</th>
<th>Description</th>
<th>Package Size</th>
<th>Configuration (words x bits)</th>
<th>Speed</th>
<th>VDD, VDDQ</th>
<th>Operating Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>D2516EC4BXGGB</td>
<td>4Gb</td>
<td>96 ball FBGA DDR3/3L 9.0x13.5x1.2</td>
<td>256Mx16</td>
<td>1600 Mbps</td>
<td>1.35V*</td>
<td>0°C ~ +95°C</td>
<td></td>
</tr>
<tr>
<td>D5128EETBPGGBU</td>
<td>4Gb</td>
<td>78 ball FBGA DDR3/3L 9.0x10.6x1.2</td>
<td>512Mx8</td>
<td>1600 Mbps</td>
<td>1.35V*</td>
<td>0°C ~ +95°C</td>
<td></td>
</tr>
<tr>
<td>D2516ECMDXGJD</td>
<td>4Gb</td>
<td>96 ball FBGA DDR3L 7.5x13.5x1.2</td>
<td>256Mx16</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>0°C ~ +95°C</td>
<td></td>
</tr>
<tr>
<td>D5128ECMDPGJD</td>
<td>4Gb</td>
<td>78 ball FBGA DDR3L 7.5x10.6x1.2</td>
<td>512Mx8</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>0°C ~ +95°C</td>
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</tr>
<tr>
<td>D2516ECMDXGME</td>
<td>4Gb</td>
<td>96 ball FBGA DDR3L 7.5x13.5x1.2</td>
<td>256Mx16</td>
<td>2133 Mbps</td>
<td>1.35V*</td>
<td>0°C ~ +95°C</td>
<td></td>
</tr>
</tbody>
</table>

*Backward compatible to 1.5V VDD, VDDQ

**Key Features**

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver
- DOS is edge-aligned with data for READS; center-aligned with data for WRITES
- Differential clock inputs (CK and !CK)
- DLL aligns DQ and DOS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODD for better signal quality
  — Synchronous ODT
  — Dynamic CDT
  — Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DO drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for Power-up sequence and reset function
- SRT range: Normal/extended
- Programmable Output driver impedance control