i-Temp DRAM

Kingston i-Temp DDR3/3L DRAM for embedded applications

Kingston on-board DRAM is designed to meet the needs of embedded applications and offers a low-voltage option for lower power consumption.
**MARKET SEGMENTS**

- **Industrial IoT / Robotics & Factory Automation**
- **5G Networking/Telecommunications Communication Modules (WiFi Routers and Mesh Devices)**
- **Wearables (Smart Watches, Health Monitors, AR & VR)**
- **Smart Home (Sound Bars, Thermostats, Fitness Equipment, Vacuums, Beds, Faucets)**
- **Smart City (HVAC, Lighting, Power Monitoring/Metering, Parking Meters)**

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**i-Temp DDR3/3L PART NUMBERS AND SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Capacity</th>
<th>Description</th>
<th>Package</th>
<th>Configuration (Words x Bits)</th>
<th>Speed Mbps</th>
<th>VDD, VDDQ</th>
<th>Operating Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1216ECMDXGI</td>
<td>2Gb</td>
<td>DDR3/3L 7.5x13.5x1.2</td>
<td>96 ball FBGA DDR3/3L</td>
<td>128Mx16</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
<tr>
<td>D2568ECMDPGI</td>
<td>2Gb</td>
<td>DDR3/3L 7.5x10.6x1.2</td>
<td>78 ball FBGA DDR3/3L</td>
<td>256Mx8</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
<tr>
<td>D2516ECMDXGI</td>
<td>4Gb</td>
<td>DDR3/3L 7.5x13.5x1.2</td>
<td>96 ball FBGA DDR3/3L</td>
<td>256Mx16</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
<tr>
<td>D5128ECMDPGI</td>
<td>4Gb</td>
<td>DDR3/3L 7.5x10.6x1.2</td>
<td>78 ball FBGA DDR3/3L</td>
<td>512Mx8</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
<tr>
<td>D2516ECMDXGMEI</td>
<td>4Gb</td>
<td>DDR3/3L 7.5x13.5x1.2</td>
<td>96 ball FBGA DDR3/3L</td>
<td>256Mx16</td>
<td>2133 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
<tr>
<td>D5116ECMDXGJDI</td>
<td>8Gb</td>
<td>DDR3/3L 9x13.5x1.2</td>
<td>96 ball FBGA DDR3/3L</td>
<td>512Mx16</td>
<td>1866 Mbps</td>
<td>1.35V*</td>
<td>-40°C ~ +95°C</td>
</tr>
</tbody>
</table>

*Backward compatible to 1.5V VDD, VDDQ*

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**KEY FEATURES**

- Double Data Rate architecture: two data transfers per clock cycle
- High-speed data transfer is realized by 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver
- DOS is edge-aligned with data for READS; center-aligned with data for WRITES
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DOS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODD for better signal quality)
  - Synchronous ODT
  - Dynamic CDT
  - Asynchronous ODT
- Multi-Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for power-up sequence and reset function
- SRT range: normal/extended
- Programmable output driver impedance control