DRAM

Kingston LPDDR4/LPDDR4x DRAM for embedded applications

Kingston discrete LPDDR4/LPDDR4x DRAM is designed to meet the needs of embedded applications and offers a high-speed option with lower power consumption.

MARKET SEGMENTS

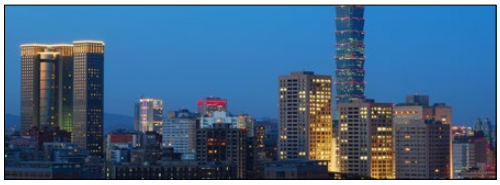

Industrial IoT / Robotics & Factory Automation


Office Equipment, Medical Devices, ATM, Vending Machines


Smart Home (Sound Bars, Thermostats, Fitness Equipment, Vacuums, Beds, Faucets)


5G Networking/Telecommunications Communication Modules (WiFi Routers and Mesh Devices)


Mobile Applications, Handheld


Smart City (HVAC, Lighting, Power Monitoring/ Metering, Parking Meters)

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KEY FEATURES

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for
  capturing data at the receiver
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Data mask (DM) write data-in at the both rising and falling edges of the data strobe
- Write Cycle Redundancy Code (CRC) is supported
- Programmable preamble for read and write is supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Driver strength selected by MRS
- Dynamic On Die Termination supported
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- This product in compliance with the RoHS directive
- Internal Vref DQ level generation is available
- TCAR (Temperature Controlled Auto Refresh) mode is supported
- LP ASR (Low Power Auto Self Refresh) mode is supported
- Command Address (CA) Parity (command/address) mode is supported
- Per DRAM Addressability (PDA)
- Fine granularity refresh is supported
- Geardown Mode(1/2 rate, 1/4 rate) is supported
- Self Refresh Abort is supported
- Maximum power saving mode is supported
- Banks Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or
  different bank group accesses are available
- DMI pin support for write data masking and DBIdc functionality
- Low power consumption
- Per Bank Refresh
- Fully compliant with the JEDEC Low Power double Data Rate 4 (LPDDR4) Specification
- Partial Array Self-Refresh (PASR)
  - o Bank Masking
  - o Segment Masking
- Auto Temperature Compensated Self-Refresh
  - o (ATCSR) by built-in temperature sensor
  - o All bank auto refresh and directed per bank auto refresh supported
- Double-data-rate architecture; two data transfers per one clock cycle
- Differential clock inputs (CK_t and CK_c) Bi-directional differential data strobe (DQS_tandDQS_c) Commands entered on both rising and falling CK_t edge; data and data mask referenced to both edges of DQS_t
- DMI pin support for write data masking and DBIdc functionality

LPDDR4 PART NUMBERS AND SPECIFICATIONS

COMMERCIAL TEMPERATURE

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D1621PM4CDGUI-U	16Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x0.8	512Mx32	3733 Mbps	1.1V	-25°C ~ +85°C
D1611PM3BDGUI-U	16Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x0.8	1Gx16	3733 Mbps	1.1V	-25°C ~ +85°C
C3222PM4CDGUI-U	32Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x0.8	1Gx32	3733 Mbps	1.1V	-25°C ~ +85°C
B3221PM3BDGUI-U	32Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x0.8	1Gx32	3733 Mbps	1.1V	-25°C ~ +85°C
Q6422PM3BDGVK-U	64Gb	200 ball FBGA LPDDR4 C-Temp	10x14.5x1.0	2Gx32	4266 Mbps	1.1V	-25°C ~ +85°C

INDUSTRIAL TEMPERATURE

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D1621PM4CDGUIW-U	16Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x0.8	512Mx32	3733 Mbps	1.1V	-40°C ~ +95°C
D1611PM3BDGVIW-U	16Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x0.8	1Gx16	4266 Mbps	1.1V	-40°C ~ +95°C
C3222PM4CDGUIW-U	32Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x0.8	1Gx32	3733 Mbps	1.1V	-40°C ~ +95°C
B3221PM3BDGVIW-U	32Gb	200 ball FBGA LPDDR4 I-Temp	10x14.5x0.8	1Gx32	4266 Mbps	1.1V	-40°C ~ +95°C

LPDDR4x PART NUMBERS AND SPECIFICATIONS

COMMERCIAL TEMPERATURE

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D1621XM4CDGVI-U	16Gb	200 ball FBGA LPDDR4x C-Temp	10x14.5x0.8	512Mx32	4266Mbps	0.6V	-25°C ~ +85°C
B3221XM3BDGVI-U	32Gb	200 ball FBGA LPDDR4x C-Temp	10x14.5x0.8	1Gx32	4266Mbps	0.6V	-25°C ~ +85°C
Q6422XM3BDGVK-U	64Gb	200 ball FBGA LPDDR4x C-Temp	10x14.5x1.0	2Gx32	4266Mbps	0.6V	-25°C ~ +85°C

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